PROGRAMA DE DOCTORAT EN ENGINYERIA ELECTRÒNICA UPC-UIB

CURSOS i SEMINARIS DE FORMACIÓ DOCTORAL – CURS 2011-2012

SHORT COURSE: **LOW-NOISE LOW-POWER WIDEBAND RECEIVERS: FRONT-END AND DIGITIZERS**

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COURSE DESCRIPTION:

Strong demand for multi-standard receivers encouraged the scientific community to find architectural solutions to maximize the SOC integration and reduce the bill of material (BOM). Direct-conversion receivers have been widely adopted in state-of-the-art wireless communication systems for their higher level of integration and baseband reconfigurability. Nonetheless, its critical drawbacks such as 1/f noise, DC-offset, and high requirement for matching still prove challenging and mandate both system- and circuit-level remedies.

The CMOS technology trend towards aggressive scaling reduces area and power consumption with high enough ft to accommodate most of the existing commercial applications under 10 GHz. Compatibility with the digital part of the transceiver mandates the use of advanced (scaled down) CMOS process. However, deep sub-micron CMOS transistors generate more flicker noise (1/f noise) than conventional CMOS process and the only way to mitigate the low-frequency noise from device perspective is to increase the device size, but this approach does not take full advantage of scaled CMOS process properties. The most promising way to alleviate the 1/f noise issue is to have zero DC current in the switching core. The passive mixer shows order of magnitude lower flicker noise compared to the Gilbert-cell mixer which requires DC current. The receiver architecture based on a single low-noise trans-conductance amplifier (LNTA) driving a current-mode passive mixer loaded by a low-impedance trans-impedance closed-loop amplifier has been widely adopted recently due to its beneficial feature in terms of noise and linearity. The architecture shows a drastic reduction in flicker noise due to the current-mode passive

mixer devoid of static current. Regarding linearity, it is improved thanks to the use of TIA's small input impedance property. Out-of-band interference (OBI) performance is improved by avoiding large voltage swing before the signal experiences first-order low-pass filtering via the I-V conversion on TIA.

However, the design of a broadband receiver based on the above architecture remains challenging in several aspects. Frequency-dependent input impedance of TIA deserves a careful attention as well, especially when used in wideband systems. The feedback gain drops at higher frequencies with the increase in virtual-ground impedance. In this course, we present a broadband, low-power, low-cost receiver front-end with a dual feedback CG-LNTA driving a current-mode passive mixer loaded by a virtual-ground generated by a wideband feed-forward-compensated TIA. The CG-LNTA utilizes capacitor cross-coupling and positive feedback from the cascode node of the amplifier such that the LNTA can overcome the design trade-off among input impedance, trans-conductance gain, and LNTA load impedance.

In addition to the front-end issues, another challenge is the processing of the down-converted information through a programmable gain amplifier, band-limited filter and ADC. The design trade-offs will be further analyzed. Specifically, the trade-offs between filter order and ADC resolution is studied. The design of a receiver for digital TV applications is used as a case of study. Filter design issues as well as fundamentals on both pipeline and oversampled ADCs are covered.

PROGRAM:

DAY1: Tuesday 29th May, 2012, 10:00 – 12:00h, Aula de Postgrau, 116, Edifici C5, Campus Nord UPC, Barcelona (http://maps.upc.edu/)

- Receiver Architectures
- Low-Noise Amplifiers
- Linearity Issues
- Low-Noise and low-Power Broadband Solutions

DAY2: Wednesday 30th May, 2012, 10:00 – 12:00h, Aula de Postgrau, 116, Edifici C5, Campus Nord UPC, Barcelona (http://maps.upc.edu/)

- RF Mixers
- Trans-impedance amplifiers
- Broadband Design Issues

DAY3: Thursday 31st May, 2012, 10:00 – 12:00h, Aula de Postgrau, 116, Edifici C5, Campus Nord UPC, Barcelona (http://maps.upc.edu/)

- IF Filters: Advantages and Tradeoffs
- Design requirements of the ADC-Filter interface
- Case of study: A TV Tuner Receiver for Digital TV Applications

DAY4: Friday 1st June, 2012, 10:00 – 12:00h, Aula de Postgrau, 116, Edifici C5, Campus Nord UPC, Barcelona (http://maps.upc.edu/)

- Continuous-Time ADCs: Fundamentals
- Continuous-Time ADCs: Design issues for Broadband applications
- Open issues
- Pipeline ADCs

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